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FISH & RICHARDSON, PC
12390 EL CAMINO REAL
SAN DIEGO, CA 92130-2081

EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,235	WANG ET AL.	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2002 and 12 April 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims1-31 have been examined.

Papers Received

2. Receipt is acknowledged of Declaration/Power of Attorney, Petition to Correct Inventorship, Formal Drawings, and Change of Address papers submitted, where the papers have been placed of record in the file.

Specification

3. The disclosure is objected to because of the following informalities: The headings of each section should not be underlined or in boldface type as described in 37 CFR 1.77(c). Also, there is no summary section in the specification as required by MPEP 608.01(a).

Appropriate correction is required.

4. The abstract of the disclosure is objected to because the acronym DAG is used without any definition of the term. The abstract must be understood when it stands alone. Correction is required. See MPEP § 608.01(b).

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Trace Cache of the Form of a Directed Acyclic Graph and Method of Constructing Such.

Drawings

6. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description:

414. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-5, 8-10, 16-17, 20-27 and 29-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Peled (6,073,213).

9. In regard to claim 1, Peled discloses an apparatus comprising: a cache of traces (figure 2), each trace including information about interdependent instructions among which data dependency exists (figure 3), the interdependent instructions including a criterion instruction that is part of a program sequence. Column 3, lines 37-41 show that the structure of figure 2 is of a trace cache. Figure 3 shows that the trace is made up of sequential instructions and thus are interdependent and have data dependencies with the instructions prior to them. Column 5, lines 46-48 show that each trace ends with (and thus is part of the program sequence) an instructions meeting the criteria of a branch, call, or return.

10. In regard to claim 2, Peled discloses the apparatus of claim 1 wherein the information comprises a directed acyclic graph. Figure 3, along with column 4, lines 10-33, show that the information in each trace comprises a directed acyclic graph because the trace comprises instructions with a line between other instructions showing the dependency (sequential dependency) between them and not returning to the starting instruction, which meets the definition set forth in the specification.

11. In regard to claim 3, Peled discloses the apparatus of claim 1 wherein the trace includes pointers to the interdependent instructions. Column 6, line 41 – column 7, line 19, show that the trace includes pointers to the interdependent instructions.

12. In regard to claim 4, Peled discloses the apparatus of claim 1 wherein the trace includes the interdependent instructions (figure 3).

13. In regard to claim 5, Peled discloses the apparatus of claim 1 wherein the interdependent instructions include the criterion instruction and instructions preceding the criterion instruction in the program sequence. As shown above, each trace comprises a sequence of instructions, which are the interdependent instructions. The criterion instruction is at the end of each sequence and so the sequence of instructions includes the criterion instructions and interdependent instructions preceding it.

14. In regard to claim 8, Peled discloses the apparatus of claim 1 wherein the information includes a triggering condition of the trace, the interdependent instructions of the trace being executed when the triggering condition is met. Column 8, lines 35-42, show that execution is begun (comes from idle state of the execution state machine) when the head lookup state is entered.

15. In regard to claim 9, Peled discloses the apparatus of claim 8 wherein the triggering condition includes a triggering instruction in the program sequence, the triggering condition being based on evaluation of an architectural state. Column 8, lines 38-42, show that the execution condition is a state (and thus based on it) and includes a triggering instruction in the branch that was mispredicted.

16. In regard to claim 10, Peled discloses the apparatus of claim 8 wherein the triggering condition includes a triggering instruction in the program sequence, the triggering condition being based on evaluation of a micro-architectural state. Column 8, lines 35-38, show that the execution condition mentioned above is based off of an idle state which is reached when a triggering instruction, a micro-operation branch, was mispredicted. Thus, there is a micro-architectural state to check this micro-operation condition and this is the basis for the triggering condition.

17. In regard to claim 16, Peled discloses the apparatus of claim 1 wherein traces that are data dependent of each other are chained together for serial executions. Column 3, lines 37-46, show that traces that make up multiple lines are viewed as multiple trace segments that are dependent on each other and chained together sequentially.

18. In regard to claim 17, Peled discloses the apparatus of claim 1 further comprising an instruction pointer that indexes the trace, the instruction pointer pointing to a first instruction or a last instruction of the interdependent instructions. Column 4, lines 15-33, show that there is a head and tail members (first and last instructions) of the traces.

It also shows that each member of the trace is addressed. This includes the head and tail and thus they are pointed to.

19. In regard to claim 20, Peled discloses a method comprising:

a. identifying a criterion instruction incurring latency in a program sequence; Column 5, lines 46-48, show that a branch, call, or return is identified. These instructions inherently have latency and all instructions take cycle time to complete. It states here that this instruction is the end of a trace. Column 3, lines 57-62, show that a trace comprises instructions. Figure 3 shows that a trace is in a sequence.

b. capturing the criterion instruction and instructions preceding the criterion instruction in the program sequence, the preceding instructions and the criterion instruction being interdependent; As shown above, a trace ends with a criterion instruction and therefore is preceded by the other instructions of a sequence. Figure 3 shows that these instructions are sequential and thus interdependent on each other. By being in the trace, the instructions are captured (stored) as is conventional and noted in column 1, lines 22-24.

c. and storing a trace in a trace cache, the trace including information about the criterion instruction and the preceding instructions. As shown above, the trace is stored in a trace cache. By storing the criterion and preceding instructions, the trace includes information about these instructions.

20. In regard to claim 21, Peled discloses the method of claim 20 wherein the information is in a form of a directed acyclic graph. Figure 3, along with column 4, lines

10-33, show that the information in each trace comprises a directed acyclic graph because the trace comprises instructions with a line between other instructions showing the dependency (sequential dependency) between them and not returning to the starting instruction, which meets the definition set forth in the specification.

21. In regard to claim 22, Peled discloses the method of claim 20 wherein the latency includes a long latency that exceeds a predetermined time threshold, a frequent latency that exceeds a predetermined recurrence threshold, or a long and uncertain latency that exceeds a mean threshold and a variance threshold. Column 5, line 46 - column 6, line 8, shows that a trace is terminated is if it reaches a predetermined maximum size among other conditions. If this maximum is not reached, as well as the other conditions, then the trace continues to be filled, or rebuilt. It is inherent that as a trace grows, just like an array, every time it is rebuilt, the time it takes to do so is longer. Therefore, the maximum set size given is associated with a maximum time limit. This is the predetermined long latency of a set of instructions.

22. In regard to claim 23, Peled discloses the method of claim 20 further comprising dynamically identifying the criterion instruction based on information derived from previous executions. Column 1, lines 50-53, show that a trace cache functions by storing previously executed sequences of instructions. Therefore, every instruction, including the criterion instruction, is based on a previous execution. Further proof is in column 5, lines 46-52, shows that the criterion instruction mentioned above as being a branch, call, or return can be one of multiple instances of this instruction. This means

that in order to know which instruction is the actual criterion instruction, information from previous execution must be used.

23. In regard to claim 24, Peled discloses the method of claim 20 further comprising capturing the criterion instruction and the preceding instructions by a buffer. Figure 2, shows that fill buffers (250) are used to capture, or fill, the traces.

24. In regard to claim 25, Peled discloses the method of claim 20 further comprising locating an existing trace in the trace cache before storing the trace, the existing trace and the trace to be stored having the same first instruction or the same last instruction. Column 13, lines 50-56 show that if a block is requested, it is first looked up in the trace cache. If it is not found, then it is stored (filled). This occurs during a trace build state that is part of a state machine as shown in column 8, lines 31-35. Column 13, lines 31 column 15, line 48, show the whole process where an identical trace has been found when the head is a hit (has been found in the cache).

25. In regard to claim 26, Peled discloses the method of claim 20 further comprising rebuilding the trace after a duration of time interval that grows each time the trace is rebuilt until the duration reaches a predetermined time limit. Column 5, line 46 - column 6, line 8, shows that a trace is terminated is if it reaches a predetermined maximum size among other conditions. If this maximum is not reached, as well as the other conditions, then the trace continues to be filled, or rebuilt. It is inherent that as a trace grows, just like an array, every time it is rebuilt, the time it takes to do so is longer. Therefore, the maximum set size given is associated with a maximum time limit.

26. In regard to claim 27, Peled discloses the method of claim 20 further comprising storing, in an array, the information about the criterion instruction and the preceding instructions. Figure 2, element 220 shows a tag array that is used to store the information regarding the criterion and preceding instructions.

27. In regard to claim 29, Peled discloses a computer program residing on a computer readable medium caused to:

a. identify a criterion instruction incurring latency in a program sequence; Column 5, lines 46-48, show that a branch, call, or return is identified. These instructions inherently have latency and all instructions take cycle time to complete. It states here that this instruction is the end of a trace. Column 3, lines 57-62, show that a trace comprises instructions. Figure 3 shows that a trace is in a sequence.

b. capture the criterion instruction and instructions preceding the criterion instruction in the program sequence, the preceding instructions and the criterion instruction being interdependent; As shown above, a trace ends with a criterion instruction and therefore is preceded by the other instructions of a sequence. Figure 3 shows that these instructions are sequential and thus interdependent on each other. By being in the trace, the instructions are captured (stored) as is conventional and noted in column 1, lines 22-24.

c. and store a trace in a trace file, the trace including information about the criterion instruction, the preceding instructions, and interdependency among the criterion instruction and the preceding instructions. As shown above, the trace is

stored in a trace cache. By storing the criterion and preceding instructions, the trace includes information about these instructions.

Since the invention of Peled shows in the abstract that a processor uses instructions, the above limitations performed by the processor inherently must be caused to do so by instructions (of a computer program) that are stored in a computer-readable medium (memory).

28. In regard to claim 30, Peled discloses the computer program of claim 29 wherein an analysis window defined in the computer program causes the computer to capture the criterion instruction and preceding instructions. Since the criterion instructions and the preceding instructions are captured when the criterion instruction is discovered or analyzed, it is inherent that there is some sort of analysis window or step for detecting this criteria.

29. In regard to claim 31, Peled discloses the computer program of claim 29 wherein the computer identifies the criterion instruction by profiling the program sequence. The examiner is taking profiling to mean outlining or scanning as is consistent with the common dictionary definition since there is no definition in the specification. Therefore, since a trace is scanned for a criterion instruction before identified, the program sequence is profiled.

Claim Rejections - 35 USC § 103

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

31. Claims 6, 7, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peled in view of Simons (6,044,222).

32. In regard to claim 6,

a. Peled discloses the apparatus of claim 1. Column 6, lines 44-45 and 53-55 show that a next instruction pointer is maintained for every part of a trace segment (head, tail, and bodies) and thus to every interdependent instruction.

b. Peled does not disclose wherein the interdependent instructions are classified into subslice types, the trace including a pointer to each subslice that is formed by each type of the interdependent instructions.

c. Simons has shown in figure 1a dependency graph showing the interdependencies between the two instructions. Figure 4 shows more complex dependence graphs described by the brief description of it and the preceding drawings. This figure shows that x and w are executed in parallel because they are of different types, floating point and integer respectively. This causes two subslices to be formed. These subslices will have pointers two them because as shown above, all instructions in the trace do.

d. The above shows that two different instructions types are executed in parallel. Column 5, lines 47-51, show that Simons' goal is to rearrange instructions (which is done with parallel execution) so that overall completion time is minimized. This minimization in completion time would have motivated one of

ordinary skill to modify Peled to schedule with subslices for parallel execution as taught by Simons.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Peled to execute instructions in parallel using subslices as taught by Simons.

33. In regard to claim 7, Peled in view of Simons discloses the apparatus of claim 6 wherein each subslice is stored as dependent pieces. As shown in figure 4 (left) of Simons, the subslices of w and x are dependent on instruction y and since the trace cache of Peled stores dependencies, the subslices are stored as dependent pieces.

34. In regard to claim 28,

a. Peled discloses the method of claim 27

b. Peled does not disclose wherein the array further includes a subslice type for each of the instructions, the subslice type being a result of classifying the instructions.

c. Simons has shown in figure 1a dependency graph showing the interdependencies between the two instructions. Figure 4 shows more complex dependence graphs described by the brief description of it and the preceding drawings. This figure shows that x and w are executed in parallel because they are of different types (as a result of classifying), floating point and integer respectively. This causes two subslices to be formed. Since the array stores the information regarding the criterion and preceding instructions, it would also store such subslice information.

d. The above shows that two different instructions types are executed in parallel. Column 5, lines 47-51, show that Simons' goal is to rearrange instructions (which is done with parallel execution) so that overall completion time is minimized. This minimization in completion time would have motivated one of ordinary skill to modify Peled to schedule with subslices for parallel execution as taught by Simons.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Peled to execute instructions in parallel using subslices as taught by Simons.

35. Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peled in view of Killian (6,092,187).

36. In regard to claim 11,

a. Peled discloses the apparatus of claim 1.

b. Peled does not disclose wherein the information further includes a confidence metric of the trace that predicts the likelihood of producing a correct result from executing the trace.

c. Killian has shown in column 5, lines 32-36, that a trace cache uses confidence levels (metrics). These confidence levels predict the likelihood of producing a correct prediction as shown in column 3, lines 59-65. Killian shows in lines 64-65 that a larger confidence value yields greater confidence in a prediction.

d. It is well known in the art that greater confidence in a prediction is desirable. This greater confidence would have motivated one of ordinary skill in the art to modify the design of Peled to use the confidence levels taught by Killian.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Peled to include the confidence level system taught by Killian so that greater confidence in the instruction predictions of traces can be realized.

37. In regard to claim 12, Peled in view of Killian discloses the apparatus of claim 11 wherein the confidence metric of the trace indicates whether or not the trace should be replaced by a new trace storing information about different instructions. The confidence level system taught by Killian shows in column 5, lines 16-31, that if a prediction is not acceptable (low confidence) a second predictor replaces it. Since the trace cache is controlled by the confidence levels and predictions are made by the traces, if the predictor is changed, that means the trace and all its instructions are replaced with new ones.

38. In regard to claim 13, Peled in view of Killian discloses the apparatus of claim 11 wherein the confidence metric of the trace indicates whether or not the trace should be rebuilt using new information about the criterion instruction that arrives at the trace cache. The confidence level system taught by Killian shows in column 5, lines 16-31, that if a prediction is not acceptable (low confidence) a second predictor replaces it. Since the trace cache is controlled by the confidence levels and predictions are made by the traces, if the predictor is changed, that means the trace and all its instructions are

replaced with new ones. Thus the trace that is sent for execution must be replaced or rebuilt. Since all traces use information from the criterion instruction to know where the trace ends. The trace is rebuilt using information from this criterion instruction.

39. In regard to claim 14, Peled in view of Killian discloses the apparatus the apparatus of claim 11 further comprising a counter having a counter value that indicates the number of times the trace has been executed, the counter value, when exceeding a frequency threshold of the trace, triggering the trace to be rebuilt. Column 15, lines 56-59 of Killian show the use of counters for prediction as taught in the background. Here in column 3, lines 59-67, it is shown that a suggested confidence level measure is using a counter to keep track of the number of executions of the trace without a misprediction. The threshold here is zero. When a misprediction is encountered the counter is reset to zero and the more correct predictions the higher the confidence level. The confidence level system taught by Killian shows in column 5, lines 16-31, that if a prediction is not acceptable (low confidence) a second predictor replaces it. Since the trace cache is controlled by the confidence levels and predictions are made by the traces, if the predictor is changed, that means the trace and all its instructions are replaced with new ones. With the confidence level surpassing the threshold at zero, there is no confidence and a different predictor (trace) will be selected or rebuilt for execution.

40. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peled in view of Ferreira de Souza.

41. In regard to claim 15,

a. Peled discloses the apparatus of claim 1

b. Peled does not disclose wherein traces that are independent of each other and adjacent in the program sequence are grouped into a very-long-instruction-word for parallel executions.

c. Ferreira de Souza discloses in section 1 that all traces are scheduled into VLIW (very-long-instruction-word) instructions for execution. This means that traces independent of each other in the program sequence are grouped into VLIW instructions. Since it is also shown here that VLIW machines execute operations in parallel.

d. The introduction section of Ferreira de Souza also shows that by converting these traces into VLIW instructions, VLIW performance and simplicity is attained. This performance and simplicity would have motivated one of ordinary skill in the art to modify the design of Peled to group traces into VLIW instructions as taught by Ferreira de Souza.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Peled to group traces into VLIW instructions as taught by Ferreira de Souza to increase performance and simplicity.

42. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peled in view of Schwarz (4,916,652).

43. In regard to claim 18,

a. Peled discloses the apparatus of claim 1 comprising a main pipeline executing the program sequence. Figure 1 shows that because the processor has decode and execution units, it is pipelined and thus has a main pipeline.

b. Peled does not disclose the apparatus further comprising at least one secondary pipeline disjoint from the main pipeline executing the interdependent instructions.

c. Schwarz has disclosed in column 1, line 66 – column 2, line 3 the use of disjoint multiple pipelines for executing multiple instructions at once.

d. By using the multiple pipelines taught by Schwarz in the design of Peled, the problem introduced by Schwarz in column 1, lines 47-55 of having to wait for each instruction stream to finish before a second could start. One of ordinary skill in the art would recognize this to save processing time because of parallel execution. This faster processing would have motivated one of ordinary skill in the art to modify the design of Peled to include the multiple pipelines of Schwarz.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Peled to incorporate the multiple pipeline scheme taught by Schwarz so that processing time is reduced.

44. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peled in view of Davis.

45. In regard to claim 19,

a. Peled discloses the apparatus of claim 1 wherein the program sequence is executed by a main thread on a pipeline. Figure 1 shows that because the processor has decode and execution units, it is pipelined and thus has a main pipeline.

b. Peled does not disclose wherein the interdependent instructions are executed by a secondary thread on the same pipeline,

c. Davis has disclosed in figure 1 a processor that has two threads (elements 28) processed in the same pipeline. Column 2, lines 12-41 show that multiple series of instructions are executed with these threads. Thus a program sequence and its independent instructions are processed in a main and secondary thread.

d. In column 2, lines 1-9, of Davis it is shown that using multiple threads allows for simultaneous instruction paths to execute. This simultaneous execution would have motivated one of ordinary skill in the art at the time of invention to modify the design of Peled to include the multiple threading taught by Davis.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Peled to include the multiple thread processing taught by Davis so that instruction threads may be executed in parallel and processing time sped up.

Conclusion

46. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

47. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents and paper are cited to further show the art with respect to trace caches and directed acyclic graphs.

US Pat No 5,937,195 to Ju discloses a method for predicated code involving traces that are modeled after acyclic graphs.

US Pat No 6,594,824 to Volkonsky discloses trace structure where the basic blocks stored therein are formed from a directed acyclic graph.

Assigning Confidence to Conditional Branch Predictions to Jacobsen, Rotenberg, and Smith teaches how to assign confidence levels to predictions using counters.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7305. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703)872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Shane F Gerstl
Examiner
Art Unit 2183

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

SFG
January 8, 2004